CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An integrated magnetoresistive semiconductor memory, comprising:

a plurality of memory cells, each one of said plurality of said memory cells including a thin tunnel barrier, two magnetic layers isolated by said tunnel barrier, and an activatable isolating element ~~selected from the group consisting~~ formed of a switching transistor ~~and a diode~~;

integrated connecting conductors including word lines, digit lines, bit lines and at least one line for activating said activatable isolating element of at least one of said plurality of said memory cells;

two metallization planes; and

a polysilicon connection plane;

each one of said connecting conductors being located in a plane selected from the group consisting of said two metallization planes and said polysilicon connection plane.

Claim 2 (previously presented): The integrated magnetoresistive semiconductor memory according to claim 1, wherein said digit lines and said word lines are situated in a given one of said two metallization planes.

Claim 3 (previously presented): The integrated magnetoresistive semiconductor memory according to claim 1, wherein said word lines are low-resistance word-lines.

Claim 4 (previously presented): The integrated magnetoresistive semiconductor memory according to claim 1, wherein ones of said connecting conductors that are located in said polysilicon connection plane serve as a substrate short circuit.

Claim 5 (currently amended): A method for fabricating an integrated magnetoresistive semiconductor memory, which comprises:

providing an integrated magnetoresistive semiconductor memory including a plurality of memory cells;

for each one of the memory cells, providing two magnetic layers that are isolated by a thin tunnel barrier;

for each one of the memory cells, providing an activatable isolating element ~~selected from the group consisting~~ formed of a switching transistor ~~and a diode~~;

providing the integrated magnetoresistive semiconductor memory with integrated connecting conductors including word lines, digit lines, bit lines and lines for activating the activatable isolating element of each one of the plurality of the memory cells;

providing each one of the connecting conductors in a plane selected from the group consisting of two metallization planes and a polysilicon connection plane;

providing the digit lines in a given one of the metallization planes;

providing first lines in the given one of the metallization planes and in the polysilicon connection plane; and

using the first lines, which have not yet been used in a layout of the magnetoresistive semiconductor memory, for connecting other elements of the magnetoresistive semiconductor memory.

Claim 6 (previously presented): The fabrication method according to claim 5, which comprises using the given one of the metallization planes for the word lines.

Claim 7 (previously presented): The fabrication method according to claim 6, which comprises providing the word lines as low resistance word lines.

Claim 8 (previously presented): The fabrication method according to claim 5, which comprises using the polysilicon connection plane as a substrate short circuit.